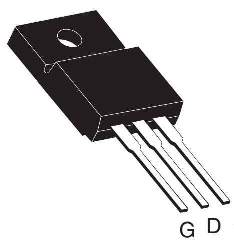
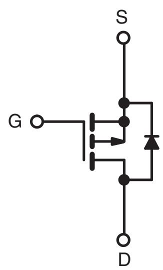
# Power MOSFET

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$ (V) | - 250 | |
| $R_{DS(on)}$ (Ω) | $V_{GS}$ = - 10 V | 1.0 |
| $Q_g$ (Max.) (nC) | 38 | |
| $Q_{gs}$ (nC) | 8.0 | |
| $Q_{gd}$ (nC) | 18 | |
| Configuration | Single | |

TO-220 FULLPAK




P-Channel MOSFET

## FEATURES

- Advanced Process Technology
- Dynamic dV/dt Rating
- 150 °C Operating Temperature
- Fast Switching
- P-Channel
- Fully Avalanche Rated
- Lead (Pb)-free Available

RoHS*
COMPLIANT

## DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.
The TO-220 FULLPAK eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The FULLPAK is mounted to a heatsink using a single clip or by a single screw fixing.

| ORDERING INFORMATION | |
|---|---|
| Package | TO-220 FULLPAK |
| Lead (Pb)-free | IRFI9634GPbF |
| | SiHFI9634G-E3 |
| SnPb | IRFI9634G |
| | SiHFI9634G |

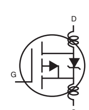
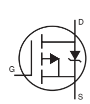
**ABSOLUTE MAXIMUM RATINGS** $T_C$ = 25 °C, unless otherwise noted

| PARAMETER | | | SYMBOL | LIMIT | UNIT |
|---|---|---|---|---|---|
| Drain-Source Voltage | | | $V_{DS}$ | - 250 | V |
| Gate-Source Voltage | | | $V_{GS}$ | ± 20 | |
| Continuous Drain Current | $V_{GS}$ at - 10 V | $T_C$ = 25 °C | $I_D$ | - 4.1 | A |
| | | $T_C$ = 100 °C | | - 2.6 | |
| Pulsed Drain Current[a] | | | $I_{DM}$ | - 31 | |
| Linear Derating Factor | | | | 0.16 | W/°C |
| Single Pulse Avalanche Energy[b] | | | $E_{AS}$ | 520 | mJ |
| Repetitive Avalanche Current[a] | | | $I_{AR}$ | - 4.1 | A |
| Repetitive Avalanche Energy[a] | | | $E_{AR}$ | 3.5 | mJ |
| Maximum Power Dissipation | $T_C$ = 25 °C | | $P_D$ | 35 | W |
| Peak Diode Recovery dV/dt[c] | | | dV/dt | - 5.0 | V/ns |
| Operating Junction and Storage Temperature Range | | | $T_J$, $T_{stg}$ | - 55 to + 150 | °C |
| Soldering Recommendations (Peak Temperature) | for 10 s | | | 300[d] | |
| Mounting Torque | 6-32 or M3 screw | | | 10 | lbf · in |
| | | | | 1.1 | N · m |

**Notes**
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Starting $T_J$ = 25 °C, L = 62 mH, $R_G$ = 25 Ω, $I_{AS}$ = - 4.1 A (see fig. 12).
c. $I_{SD} \leq$ - 4.1 A, dI/dt $\leq$ - 640 A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 150 °C.
d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

| THERMAL RESISTANCE RATINGS | | | | |
|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TYP.** | **MAX.** | **UNIT** |
| Maximum Junction-to-Ambient | $R_{thJA}$ | - | 65 | °C/W |
| Maximum Junction-to-Case (Drain) | $R_{thJC}$ | - | 3.6 | |

| **SPECIFICATIONS** $T_J$ = 25 °C, unless otherwise noted | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 µA | - 250 | - | - | V |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to 25 °C, $I_D$ = 1 mA | - | - 0.27 | - | V/°C |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | - 2.0 | - | - 4.0 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{GS}$ = ± 20 V | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = - 250 V, $V_{GS}$ = 0 V | - | - | - 25 | µA |
| | | $V_{DS}$ = - 200 V, $V_{GS}$ = 0 V, $T_J$ = 150 °C | - | - | - 250 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = - 10 V; $I_D$ = - 2.5 A[b] | - | - | 1.0 | Ω |
| Forward Transconductance | $g_{fs}$ | $V_{DS}$ = - 50 V, $I_D$ = - 4.1 A[b] | 2.2 | - | - | S |
| **Dynamic** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = - 25 V, f = 1.0 MHz, see fig. 5 | - | 680 | - | pF |
| Output Capacitance | $C_{oss}$ | | - | 170 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 40 | - | |
| Drain to Sink Capacitance | C | f = 1.0 MHz | - | 12 | - | |
| Total Gate Charge | $Q_g$ | $V_{GS}$ = - 10 V; $I_D$ = - 4.1 A, $V_{DS}$ = - 200 V, see fig. 6 and 13[b] | - | - | 38 | nC |
| Gate-Source Charge | $Q_{gs}$ | | - | - | 8.0 | |
| Gate-Drain Charge | $Q_{gd}$ | | - | - | 18 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = - 130 V, $I_D$ = - 4.1 A, $R_G$ = 12 Ω, $R_D$= 31 Ω, see fig. 10[b] | - | 12 | - | ns |
| Rise Time | $t_r$ | | - | 23 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 34 | - | |
| Fall Time | $t_f$ | | - | 21 | - | |
| Internal Drain Inductance | $L_D$ | Between lead, 6 mm (0.25") from package and center of die contact  | - | 4.5 | - | nH |
| Internal Source Inductance | $L_S$ | | - | 7.5 | - | |
| **Drain-Source Body Diode Characteristics** | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | MOSFET symbol showing the integral reverse p - n junction diode  | - | - | - 4.1 | A |
| Pulsed Diode Forward Current[a] | $I_{SM}$ | | - | - | - 16 | |
| Body Diode Voltage | $V_{SD}$ | $T_J$ = 25 °C, $I_S$ = - 4.1 A, $V_{GS}$ = 0 V[b] | - | - | - 6.5 | V |
| Body Diode Reverse Recovery Time | $t_{rr}$ | $T_J$ = 25 °C, $I_F$ = - 4.1 A, dI/dt = -100 A/µs[b] | - | 190 | 290 | ns |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | | - | 1.5 | 2.2 | µC |
| Forward Turn-On Time | $t_{on}$ | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$) | | | | |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

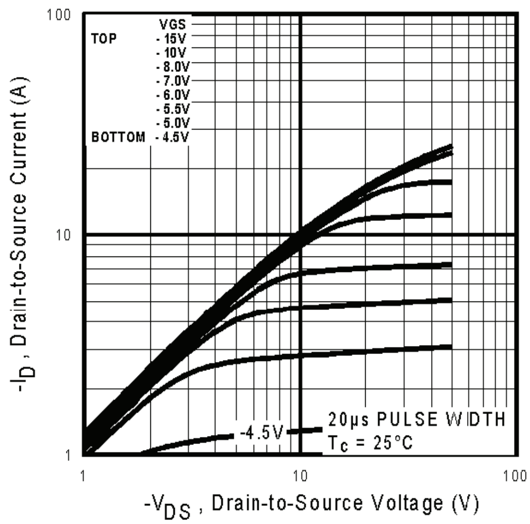



**Fig. 1 - Typical Output Characteristics, $T_C$ = 25 °C**

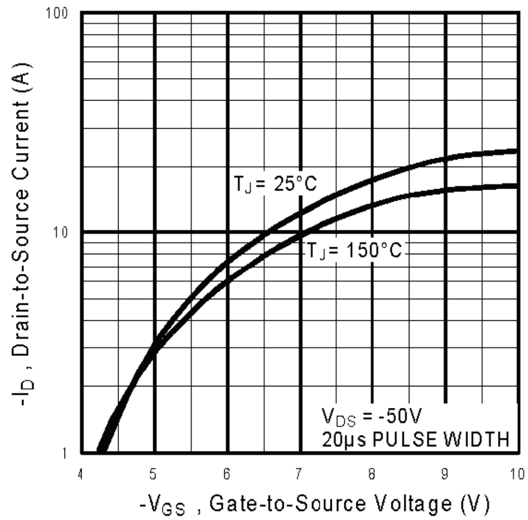



**Fig. 3 - Typical Transfer Characteristics**

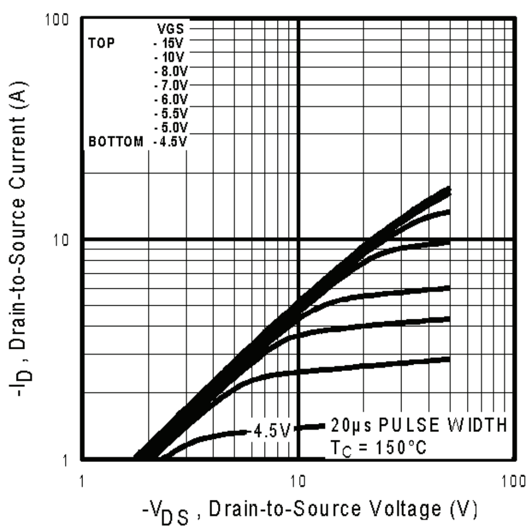



**Fig. 2 - Typical Output Characteristics, $T_C$= 150 °C**

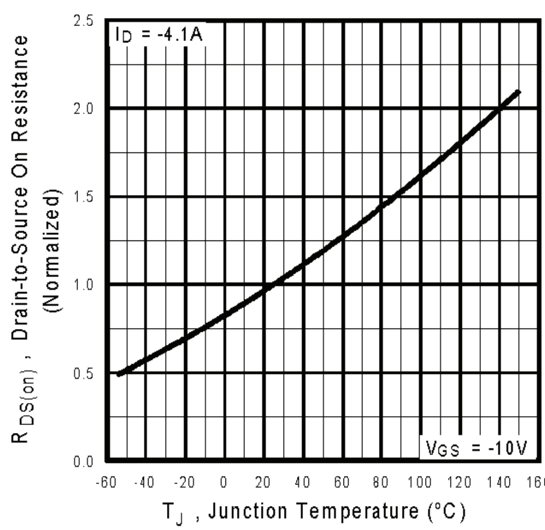



**Fig. 4 - Normalized On-Resistance vs. Temperature**

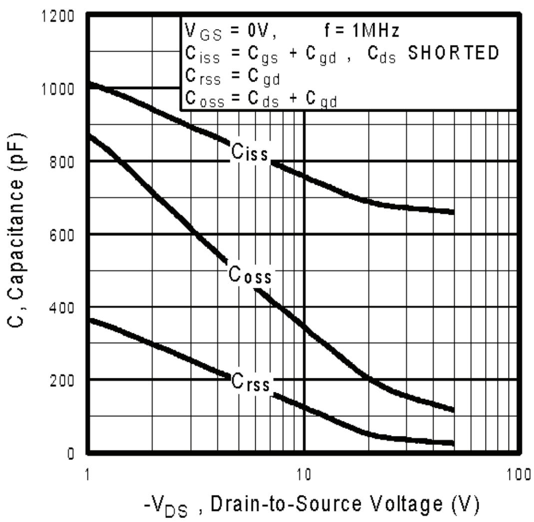



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

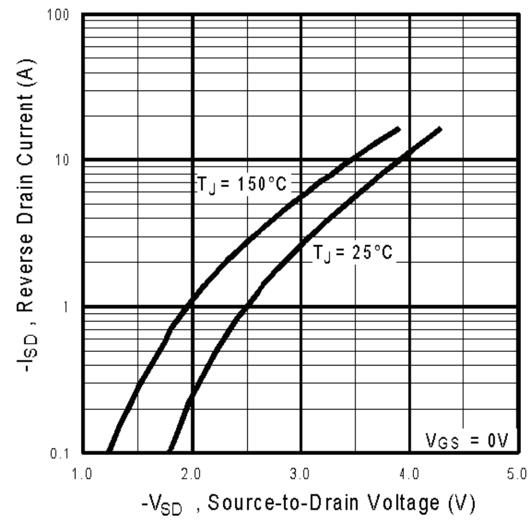



**Fig. 7 - Typical Source-Drain Diode Forward Voltage**

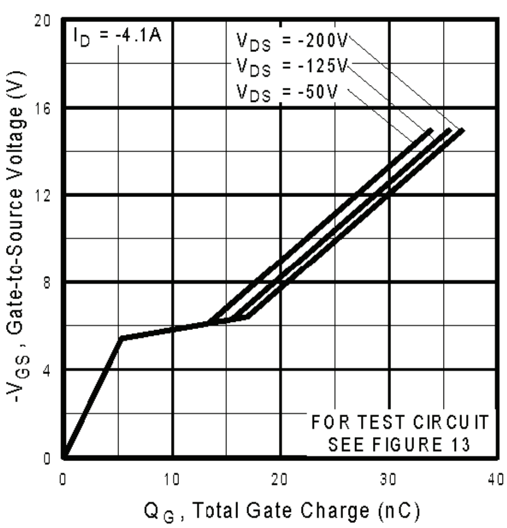



**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**

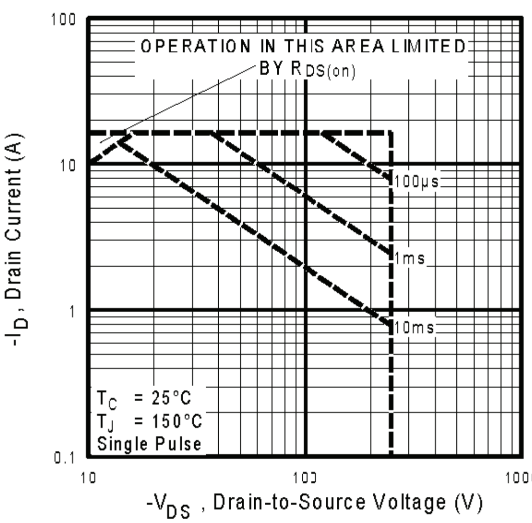



**Fig. 8 - Maximum Safe Operating Area**

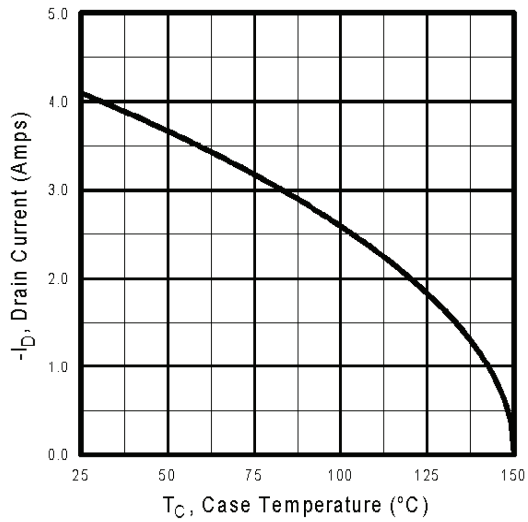



Fig. 9 - Maximum Drain Current vs. Case Temperature

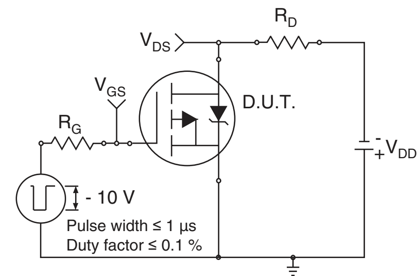



Fig. 10a - Switching Time Test Circuit

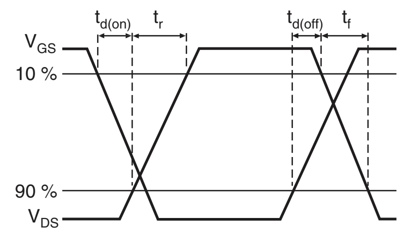



Fig. 10b - Switching Time Waveforms

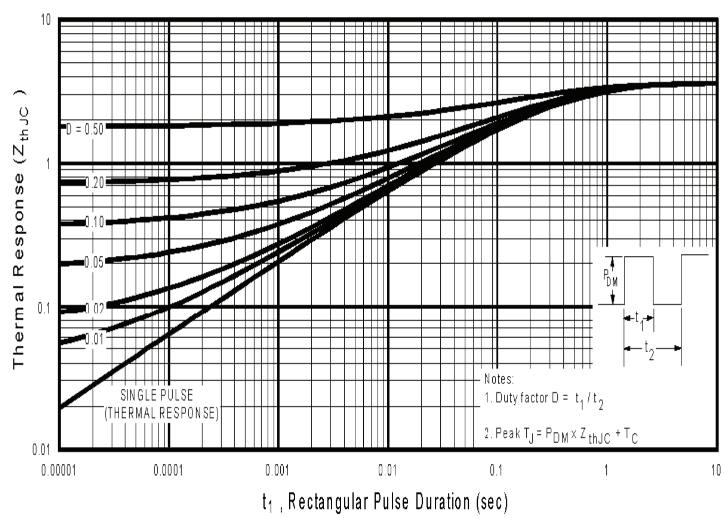



Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

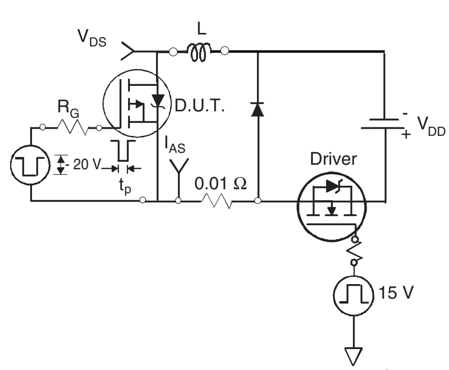



Fig. 12a - Unclamped Inductive Test Circuit

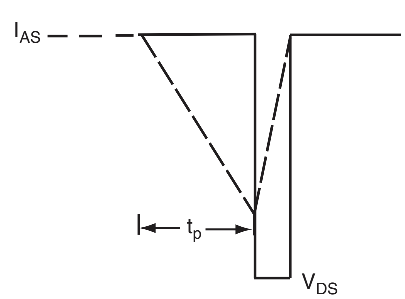



Fig. 12b - Unclamped Inductive Waveforms

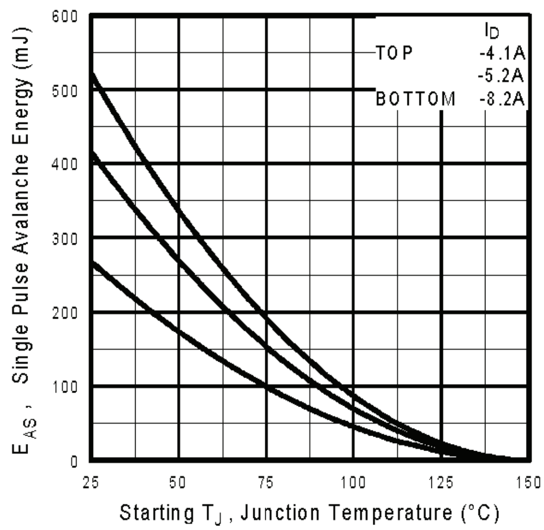



**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**

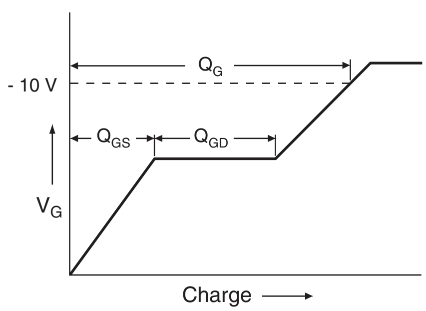



**Fig. 13a - Basic Gate Charge Waveform**

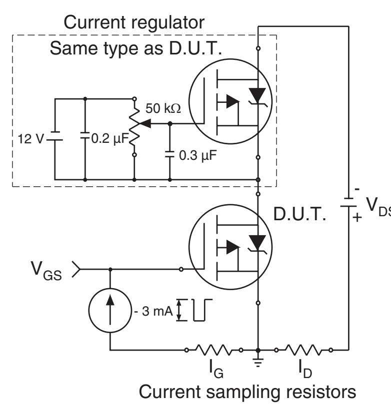
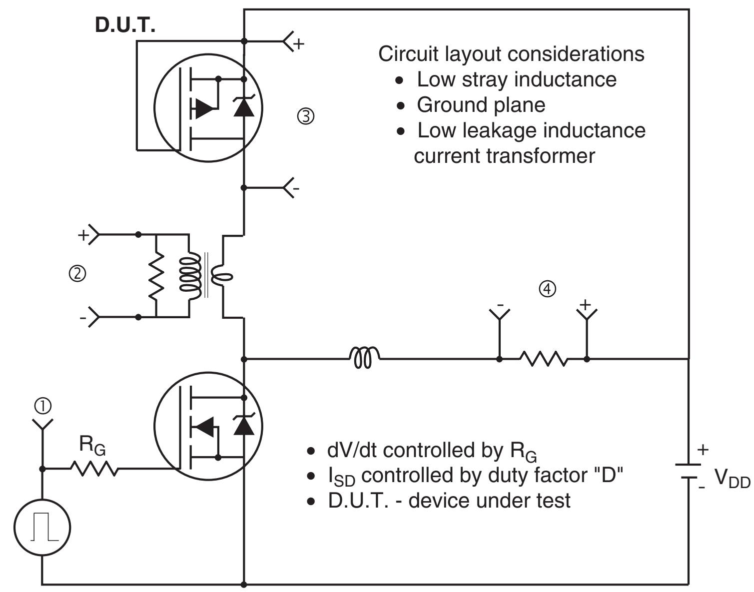
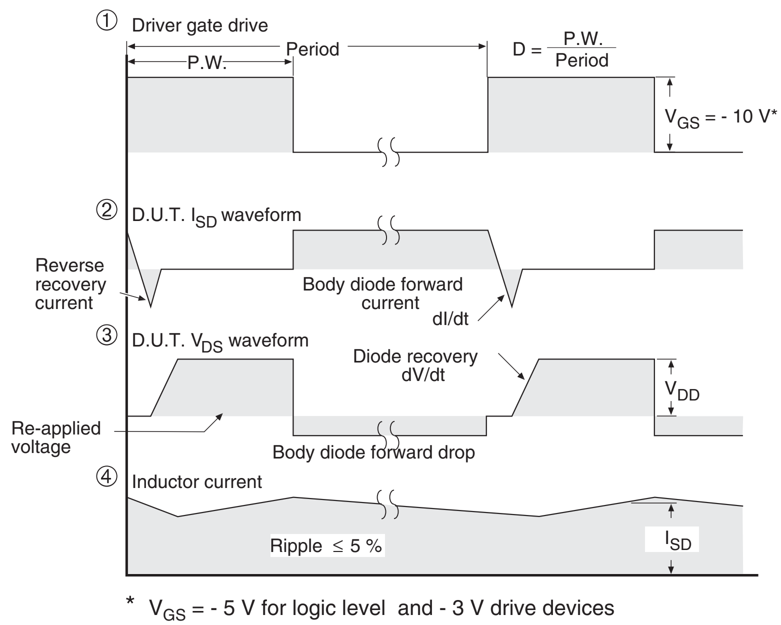



**Fig. 13b - Gate Charge Test Circuit**

## Peak Diode Recovery dV/dt Test Circuit




• Compliment N-Channel of D.U.T. for driver




* $V_{GS}$ = - 5 V for logic level and - 3 V drive devices

**Fig. 14 - For P-Channel**

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